IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A computer system comprising:

a host computer system;

a first component configured to output data, wherein the data includes requested data and unrequested data;

a second component configured to request data from the first component, wherein the second component includes a signature analysis register configured to capture data, wherein the signature analysis register is configured to be controlled by the host computer system;

a bus coupling the first component and the second component and configured to transmit data between the first component and the second component; and

a controller coupled to receive the data and the unrequested data output by the first component, wherein the controller is configured to receive the data output by the first component in response to the second component's request, wherein the controller is configured to replace the unrequested data with predictable data and to output the predictable data and the requested data, wherein the signature analysis register is configured to capture the predictable data and the requested data.

2. (Original) The computer system of claim 1, wherein the controller is configured to store an indication identifying the requested data in response to the second component requesting data from the first component, wherein the controller is configured to select which of the data output by the first component is unrequested data dependent on the indication.

3. (Original) The computer system of claim 2, wherein the indication is a mask indicating which portions of the data are valid.

4. (Original) The computer system of claim 3, wherein the controller is configured to store a plurality of masks that each correspond to one of a plurality of pending requests for data from the first component.

5. (Original) The computer system of claim 3, wherein the controller includes one or more multiplexers, wherein each multiplexer's inputs include a predictable data value and a portion of the data output by the first component, wherein each multiplexer is controlled by a portion of the mask that corresponds to the portion of the data output by the first component.

6. (Original) The computer system of claim 2, wherein each bit included in the predictable data has a logical value of zero.

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7. (Original) The computer system of claim 2, wherein the first component includes a data queue configured to buffer data before the data is output on the bus, wherein the controller is coupled to the output of the data queue, wherein the controller is configured to output the predictable data and the requested data on the bus.

8. (Original) The computer system of claim 2, wherein the second component further includes a second signature analysis register configured to capture control signals.

9. (Original) The computer system of claim 2, wherein the second component includes a data queue configured to buffer data after the data is received from the bus, wherein the controller is coupled to the input of the data queue, wherein the controller is configured to output the predictable data and the requested data to the data queue.

10. (Currently Amended) A graphics system comprising:

a first component configured to output data, wherein the data includes requested data and unrequested data;

a second component configured to request data from the first component, wherein the second component includes a signature analysis register configured to capture data;

a bus coupling the first component and the second component and configured to transmit data between the first component and the second component; and

a controller coupled to receive the requested data and the unrequested data output by the first component, wherein the controller is configured to receive the data output by the first component in response to the second component's request, wherein the controller is configured to replace the unrequested data with predictable data and to output the predictable data and the requested data, wherein the signature analysis register is configured to capture the predictable data and the requested data.

11. (Original) The graphics system of claim 10, wherein the first component includes a frame buffer and the second component includes a hardware accelerator.

12. (Original) The graphics system of claim 10, wherein the first component includes a media processor and the second component includes a hardware accelerator.

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13. (Original) The graphics system of claim 10, wherein the controller is configured to store an indication identifying the requested data in response to the second component requesting data from the first component, wherein the controller is configured to select which of the data output by the first component is unrequested data dependent on the indication.

14. (Original) The graphics system of claim 13, wherein the indication is a mask indicating which portions of the data are valid.

15. (Original) The graphics system of claim 14, wherein the controller is configured to store a plurality of masks that each correspond to one of a plurality of pending requests for data from the first component.

16. (Original) The graphics system of claim 14, wherein the controller includes one or more multiplexers, wherein each multiplexer's inputs include a predictable data value and a portion of the data output by the first component, wherein each multiplexer is

controlled by a portion of the mask that corresponds to the portion of the data output by the first component.

17. (Original) The graphics system of claim 13, wherein each bit included in the predictable data has a logical value of zero.

18. (Original) The graphics system of claim 13, wherein the first component includes a data queue configured to buffer data before the data is output on the bus, wherein the controller is coupled to the output of the data queue, wherein the controller is configured to output the predictable data and the requested data on the bus.

19. (Original) The graphics system of claim 13, wherein the second component further includes a second signature analysis register configured to capture control signals.

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20. (Original) The graphics system of claim 13, wherein the second component includes a data queue configured to buffer data after the data is received from the bus, wherein the controller is coupled to the input of the data queue, wherein the controller is configured to output the predictable data and the requested data to the data queue.

21. (Original) A method of performing signature analysis, the method comprising:

a requesting device requesting data;

a providing device providing data in response to said requesting, wherein the data comprises requested data and unrequested data;

replacing the unrequested data with predictable data, wherein the predictable data has a predictable value; and

a signature analysis register in the requesting device capturing the predictable data and the requested data.

22. (Currently Amended) The method of claim 21, further comprising storing an indication identifying the requested data in response to said requesting device requesting

data, wherein said replacing comprises selecting the unrequested data for replacement dependent on the ~~first~~ indication.

23. (Original) The method of claim 22, wherein the indication is a mask indicating which portions of the data provided by the providing device are valid.

24. (Original) The method of claim 23, further comprising storing a plurality of masks that each correspond to one of a plurality of pending requests for data.

25. (Original) The method of claim 23, wherein said replacing comprises one or more multiplexers selecting a predictable data value to output if a portion of the mask that corresponds to a first portion of the data provided by the providing device indicates that the first portion of the data is not valid.

26. (Original) The method of claim 23, wherein said replacing comprises one or more multiplexers selecting a first portion of the data provided by the providing device to output if a portion of the mask that corresponds to the first portion of the data indicates that the first portion of the data is valid.

27. (Original) The method of claim 21, wherein each bit included in the predictable data has a logical value of zero.

28. (Original) The method of claim 21, further comprising buffering the data provided by the providing device in a data queue before the data is output on a bus, wherein said replacing comprises replacing the unrequested data output from the data queue and outputting the predictable data and the requested data on the bus.